

The M20 router's compact design offers tremendous performance and port density where space is a premium. The M20 router has a rich feature set that includes numerous advantages.

- Route lookup rates in excess of 40 Mpps for wire-rate forwarding performance
- Aggregate throughput capacity exceeding 20 Gbps
- Performance-based packet filtering and sampling with the Internet Processor II ASIC
- Redundant System and Switch Board and redundant Routing Engine
- Market-leading port density and flexibility
- Space and power efficiency (both DC and 110 VAC supported)
- Production-proven routing software with Internet-scale implementations of BGP4, IS-IS, OSPF, MPLS traffic engineering, class of service, and multicasting applications

## DATASHEET

### M20 Internet Backbone Router

The M20™ Internet backbone router is a high-performance routing platform that is built for a variety of Internet applications, including high-speed access, public and private peering, hosting sites, and backbone core networks.

The M20 router leverages proven M40™ Internet backbone router technology that has been shipping and deployed in the world's

largest service provider networks since September, 1998. It runs the same JUNOS™ Internet software and shares the same interfaces that are supported by the M40 router, providing a seamless upgrade path that protects your investment. Moreover, its compact design (14 in / 35.56 cm high) delivers market-leading performance and port density, while consuming minimal rack space.



The M20 router offers wire-rate performance, advanced features, internal redundancy, and scalability in a space-efficient package.

## M20 Internet Backbone Router Advantages

Features	Benefits
Architecture	
Highly integrated ASIC forwarding	<ul style="list-style-type: none"> <li>■ Fully sized and designed to perform lookups at a rate of 40 Mpps.</li> <li>■ Scales well with large, complex forwarding tables.</li> <li>■ Full utilization of expensive circuits.</li> <li>■ Packet size does not affect forwarding performance.</li> <li>■ Rock solid system stability.</li> <li>■ Lower part count for high reliability.</li> </ul>
Routing and forwarding cleanly separated	<ul style="list-style-type: none"> <li>■ Routing fluctuations and network instability do not impede performance packet forwarding at full wire rate.</li> <li>■ Rapid convergence.</li> <li>■ Reliable and predictable performance for latency sensitive traffic, such as voice over IP and streaming video multicasting.</li> </ul>
Single-stage buffering	<ul style="list-style-type: none"> <li>■ Eliminates head-of-line blocking.</li> <li>■ Efficiently uses available interface bandwidth.</li> <li>■ Optimal support for multicast traffic.</li> <li>■ Reduces latency by requiring only one write to and one read from shared memory.</li> </ul>
Features are implemented in ASICs	<ul style="list-style-type: none"> <li>■ Industry-leading performance with value-added services enabled.</li> </ul>
Redundant System and Switch Board (SSB)	<ul style="list-style-type: none"> <li>■ Increases system availability.</li> <li>■ Ensures automatic failover to redundant SSB in case of failure.</li> </ul>
Redundant Routing Engine	<ul style="list-style-type: none"> <li>■ Increases system availability.</li> <li>■ Decreases mean time to repair (MTTR).</li> </ul>
Hot Swappable Flexible PIC Concentrators, SSBs, Routing Engines, and power supplies	<ul style="list-style-type: none"> <li>■ Increases system serviceability and availability.</li> <li>■ Decreases MTTR.</li> </ul>
JUNOS Internet software already deployed in the largest and fastest growing networks	<ul style="list-style-type: none"> <li>■ Proven performance and reliability.</li> </ul>

Performance-based packet filtering of inbound and outbound traffic based on any combination of matches

- Source IP address
- Destination IP address
- DiffServ byte
- IP protocol
- IP fragmentation offset and control fields (Offset, MF, DF)
- Source transport port
- Destination transport port
- TCP control bits (SYN, ACK, FIN)
- You can configure one input filter and one output filter for each logical interface. You can set multiple match conditions per filter, as well as configure multiple actions for each match condition.

## M20 Internet Backbone Router Advantages (continued)

Features	Benefits
<b>Performance-based IP Services (continued)</b>	
Support for Label Distribution Protocol (LDP) IETF draft (draft-ietf-mpls-ldp-05.txt) and support for optional features <ul style="list-style-type: none"> <li>■ Upstream unsolicited label distribution discipline</li> <li>■ Liberal label retention mode</li> <li>■ Neighbor discovery</li> </ul>	<ul style="list-style-type: none"> <li>■ Provides interoperability with access devices that use LDP (for example, tunneling of virtual private network traffic).</li> <li>■ Supports a core IP network that does not carry full Internet routes and where traffic engineering is not required.</li> </ul>
<b>Class of Service</b>	
Token bucket mechanism on DS-3, E3, and SONET/SDH interfaces	<ul style="list-style-type: none"> <li>■ Enables you to perform rate policing on input.</li> </ul>
Four queues per physical interface	<ul style="list-style-type: none"> <li>■ Enables you to classify all out-bound traffic into four distinct groups.</li> </ul>
Classification based on incoming logical interface, IP precedence value, or destination IP address	<ul style="list-style-type: none"> <li>■ Provides preferential traffic handling.</li> </ul>
Weighted Round Robin queue servicing based on configurable weights	<ul style="list-style-type: none"> <li>■ Enables you to assign a percentage of bandwidth to each class.</li> <li>■ Controls the amount of bandwidth each class receives on a circuit, thereby ensuring that heavy traffic demands of some classes do not adversely affect other classes.</li> <li>■ Provides preferential traffic handling.</li> </ul>
Random Early Detection congestion management	<ul style="list-style-type: none"> <li>■ Reduces the probability that congestion will occur.</li> <li>■ Minimizes packet loss and delay.</li> <li>■ Maximizes TCP throughput.</li> <li>■ Maximizes the utilization of links over time.</li> <li>■ Provides preferential traffic handling.</li> </ul>
Configurable memory allocated to each queue	<ul style="list-style-type: none"> <li>■ Gives more control over minimizing latency and the potential for congestion by configuring the amount of available bandwidth.</li> </ul>
<b>Interfaces</b>	
Market-leading port density	<ul style="list-style-type: none"> <li>■ Efficient use of POP rack space.</li> <li>■ Future growth not limited by space.</li> </ul>
Fine granularity of interchangeable interfaces	<ul style="list-style-type: none"> <li>■ Flexibly deployed in multiple environments including core, peering, high-speed access, and hosting.</li> <li>■ Lowers the cost of entry configurations.</li> </ul>
<b>Protection Mechanisms</b>	
MPLS Fast Reroute	<ul style="list-style-type: none"> <li>■ Recovers from MPLS path failures for SDH and WDM connections.</li> </ul>
Dual-router Automatic Protection Switching (APS) 1:1	<ul style="list-style-type: none"> <li>■ Ensures rapid recovery from router-to-ADM circuit failures by switching to a back-up fiber.</li> </ul>
Virtual Router Redundancy Protocol (VRRP)	<ul style="list-style-type: none"> <li>■ Leverages the inherent redundance of routers on a Gigabit Ethernet LAN.</li> </ul>
<b>Environmental</b>	
Maximum chassis power of 24 A at -48 VDC, or 12 A at 100 VAC, 6 A at 240 VAC	<ul style="list-style-type: none"> <li>■ Efficient use of POP power (&lt;1.7 Amp/rack inch).</li> <li>■ Lowers POP cooling requirements.</li> </ul>
Maximum heat dissipation of 4,000 BTU	<ul style="list-style-type: none"> <li>■ Protects against overheating.</li> </ul>

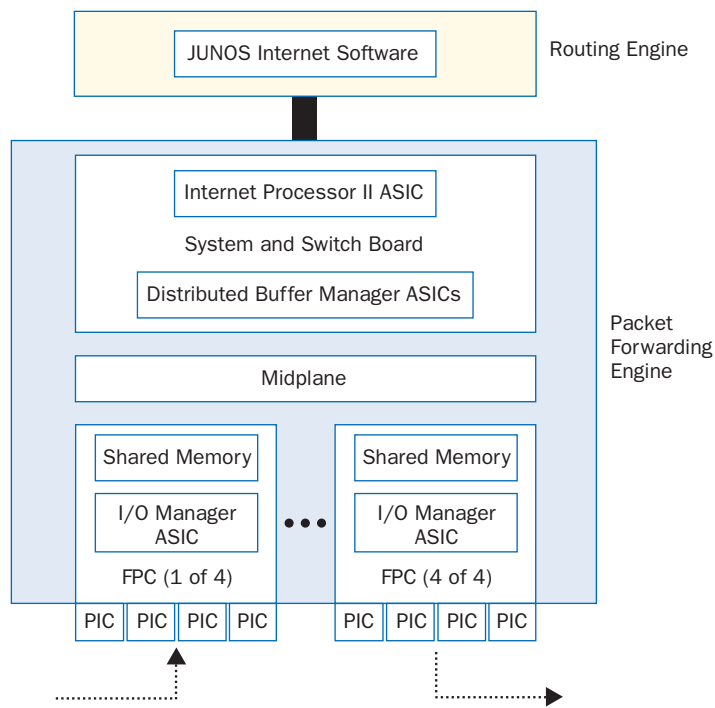
## M20 System Architecture

The two key components of the M20 architecture are the Packet Forwarding Engine (PFE) and the Routing Engine, which are connected via a 100-Mbps link.

- The PFE is responsible for packet forwarding performance. It consists of the Flexible PIC Concentrators (FPCs), physical interface cards (PICs), System and Switch Board (SSB), and state-of-the-art ASICs.
- The Routing Engine maintains the routing tables and controls the routing protocols. It consists of an Intel-based PCI platform running JUNOS software.

The architecture ensures industry-leading service delivery by cleanly separating the forwarding performance from the routing performance. This separation ensures that stress experienced by one component does not adversely affect the performance of the other since there is no overlap of required resources. Routing fluctuations and network instability do not limit the forwarding of packets. The use of ASICs ensures that the forwarding table maintains a steady state, which is particularly beneficial during times of network instability.

Logical View of M20 Architecture



### Leading-edge ASICs

The feature-rich M20 ASICs deliver a comprehensive hardware-based system for route lookups, filtering, sampling, load balancing, buffer management, switching, encapsulation, and de-encapsulation functions. To ensure a non-blocking forwarding path, all channels between the ASICs are oversized, dedicated paths.

### Internet Processor and Internet Processor II ASICs

The Internet Processor ASIC, which was originally deployed with M20 routers, supports an aggregated lookup rate of over 40 Mpps (for a routing table with 80,000 entries).

An enhanced version, the Internet Processor II ASIC, supports the same 40 Mpps lookup rate. With over one million gates, this ASIC delivers predictable, high-speed forwarding performance with service flexibility, including filtering and sampling. The Internet Processor II ASIC is the largest, fastest, and most advanced ASIC ever implemented on a router platform and deployed in the Internet.

### Distributed Buffer Manager ASIC

The Distributed Buffer Manager ASIC allocates incoming data packets throughout shared memory on the FPCs. This single-stage buffering improves performance by requiring only one write to and one read from shared memory. There are no extraneous steps of copying packets from input buffers to output buffers. The shared memory is completely nonblocking, which in turn, prevents head-of-line blocking.

### I/O Manager ASICs

The I/O Manager ASIC supports wire-rate packet parsing, packet prioritizing, and queuing. Each I/O Manager ASIC divides the packets, stores them in shared memory (managed by the Distributed Buffer Manager), and re-assembles the packets for transmission.

### Media-specific ASICs

The media-specific ASICs perform physical layer functions, such as framing. Each PIC is equipped with an ASIC or FPGA that performs control functions tailored to the PIC's media type.

- SONET/SDH Manager ASIC
- ATM Manager ASIC
- DS-3 Manager FPGA
- Gigabit Ethernet Manager ASIC

### Packet Forwarding Engine

The PFE provides Layer 2 and Layer 3 packet switching, route lookups, and packet forwarding. It forwards an aggregate of up to 40 Mpps for all packet sizes under all network conditions. The aggregate throughput is over 20 Gbps with four 3.2-Gbps full-duplex FPCs installed.

The PFE supports the same ASIC-based features supported by the M40 and M160 routers. For example, class-of-service features include policing, classification, priority queuing, Random Early Detection and Weighted Round Robin to increase bandwidth efficiency. Filtering and sampling are also available for restricting access, increasing security, and analyzing network traffic.

Finally, the PFE delivers maximum stability during exceptional conditions, while also providing a significantly lower part count. This stability reduces power consumption and increases mean time between failure.

### Flexible PIC Concentrators

The FPCs house PICs and connect them to the rest of the PFE. There is a dedicated, full-duplex, 3.2-Gbps channel between each FPC and the core of the PFE.

You can insert up to four FPCs in an M20 chassis. Each FPC slot supports one FPC or one OC-48c/STM-16 PIC. Each FPC

supports up to four of the other PICs in any combination, providing unparalleled interface density and configuration flexibility.

Each FPC contains shared memory for storing data packets received; the Distributed Buffer Manager ASIC on the SSB manages this memory. In addition, the FPC houses the I/O Manager ASIC, which performs a variety of queue management and class-of-service functions.

### Physical Interface Cards

PICs provide a complete range of fiber optic and electrical transmission interfaces to the network. The M20 router offers flexibility and conserves rack space by supporting the PICs and port densities described in the following table. All PICs occupy one of four PIC spaces per FPC (that is, they are single wide) except for the OC-48c/STM-16 PIC, which occupies an entire FPC slot (quad wide).

An additional Tunnel Services PIC enables the M20 router to function as the ingress or egress point of an IP-IP unicast tunnel, a Cisco generic routing encapsulation (GRE) tunnel, or a Protocol Independent Multicast - Sparse Mode (PIM-SM) tunnel. The Tunnel Services PIC delivers OC-12/STM-4 bandwidth, but does not have a physical interface due to its loopback function within the M20 chassis.

PIC	Port Speed	Ports / PIC	Ports / FPC Slot	Ports / Chassis	Ports / Rack
SONET/SDH					
OC-3/STM-1 SMIR	155 Mbps	4	16	64	320
OC-3/STM-1 MM	155 Mbps	4	16	64	320
OC-12c/STM-4 SMIR	622 Mbps	1	4	16	80
OC-12c/STM-4 MM	622 Mbps	1	4	16	80
OC-48c/STM-16 SMIR*	2.5 Gbps	1	1	4	20
ATM					
OC-3/STM-1 SMIR	155 Mbps	2	8	32	160
OC-12/STM-4 MM	622 Mbps	1	4	16	80
DS-3	45 Mbps	4	16	64	320
Channelized OC-12 to DS-3 SMIR	622 Mbps	1 (12 DS-3s)	4 (48 DS-3s)	16 (192 DS-3s)	80 (960 DS-3s)
E3	34 Mbps	4	16	64	320
Gigabit Ethernet LX	1 Gbps	1	4	16	80
Gigabit Ethernet SX	1 Gbps	1	4	16	80
Fast Ethernet TX	100 Mbps	4	16	64	320

\*OC-48c/STM-16 is a quad-wide interface.

LX = Long wavelength

MM = Multimode

SMIR = Single-mode, intermediate reach

SX = Short wavelength

“The way Verio views the evolution of technology in high-speed routers is today’s core technologies will eventually migrate to the edge. Juniper Networks is actually covering both ends of that issue. The M40 router is in today’s core routing technology. They are very much a leader in that area. We’re very excited to see the M20 routers for use in our regional networks that are on the edge of the backbone.”

—Chris DeMarche,  
Chief Technology  
Officer, Verio Inc.

#### System and Switch Board

The SSB performs route lookup, filtering, and sampling, as well as provides switching to the destination FPC. Hosting both the Internet Processor II ASIC and the Distributed/Buffer Manager ASIC, the SSB is responsible for making forwarding decisions, distributing data cells throughout memory, processing exception and control packets, monitoring system components, and controlling FPC resets. You can have one or two SSBs, ensuring automatic failover to a redundant SSB in case of failure.

#### Routing Engine

The Routing Engine maintains the routing tables and controls the routing protocols, as well as the JUNOS software processes that control the router’s interfaces, the chassis components, system management, and user access to the router. These routing and software processes run on top of a kernel that interacts with the PFE.

#### M20 Router Front and Back Views

- The Routing Engine processes all routing protocol updates from the network, so PFE performance is not affected.
- The Routing Engine implements each routing protocol with a complete set of Internet features and provides full flexibility for advertising, filtering, and modifying routes. Routing policies are set according to route parameters, such as prefixes, prefix lengths, and BGP attributes.

You can install a redundant Routing Engine to ensure maximum system availability and to minimize MTTR in case of failure.

#### JUNOS Internet Software

JUNOS software is optimized to scale to large numbers of network interfaces and routes. The software consists of a series of system processes running in protected memory on top of an independent operating system. The modular design improves reliability by protecting against system-wide failure since the failure of one software process does not affect other processes.

Dual Power Supplies



## Specifications

Specification	Description		
Physical	Height	14 in / 35.56 cm	
	Width	19 in / 48.26 cm	
	Depth	21 in / 53.34 cm	
	Weight	Maximum configuration 150 lbs / 60.04 kg Minimum configuration 80 lbs / 36.29 kg	
	Mounting	Front or center rack mount	
Packet Forwarding Engine	<ul style="list-style-type: none"> <li>■ Over 20-Gbps, ASIC-based packet forwarding</li> <li>■ Internet Processor II ASIC for 40-Mpps lookup</li> <li>■ Distributed Buffer Manager ASIC for coordinating pooled, single-stage buffering</li> <li>■ I/O Manager ASIC for wire-rate parsing, prioritizing, and queuing of packets</li> </ul>		
Routing Engine	<ul style="list-style-type: none"> <li>■ Compact PCI industrial form factor</li> <li>■ 333-MHz Intel Pentium II</li> <li>■ 80-MB flash drive storage</li> <li>■ 6.4-GB hard drive for secondary storage</li> <li>■ 110-MB flash PC card for tertiary storage</li> <li>■ 10/100 Ethernet port for out-of-band management</li> <li>■ Two asynchronous serial ports (RS-232) for console and remote management</li> </ul>		
Power Requirements	DC	Maximum DC Power	1,200 watts
		Maximum current	24 A at -48 VDC
		DC input voltage	-40.5 to -72 VDC operating range
		Output voltage	+3.3V, +2.5V, +5V, +24V, +12V
	AC	Maximum AC power	1,200 watts
		Maximum current	12 A at 100 VAC, 6 A at 240 VAC
		AC input voltage	100 V to 240 VAC rms
		Output voltage	+3.3V, +2.5V, +5V, +24V, +12V
Environment	Temperature	32 to 104 degrees F / 0 to 40 degrees C	
	Maximum Altitude	No performance degradation to 10,000 ft / 3,048 m	
	Relative Humidity	15 to 90 percent noncondensing	
	Shock	Tested to meet Bellcore Zone 4 earthquake requirements	
	Thermal Output	3,850 BTU/hour	
Agency Approvals	Safety	<ul style="list-style-type: none"> <li>■ CSA C22.2 No. 950 * UL 1950</li> <li>■ EN 60950, Safety of Information Technology Equipment</li> <li>■ EN 60825-1 Safety of Laser Products - Part 1: Equipment Classification, Requirements and User's Guide</li> <li>■ EN 60825-2 Safety of Laser Products - Part 2: Safety of Optical Fibre Communication Systems</li> </ul>	
	EMC	<ul style="list-style-type: none"> <li>■ AS 3548 Class A (Australia)</li> <li>■ EN 55022 Class A emissions (Europe)</li> <li>■ FCC Class A (USA)</li> <li>■ VCCI Class A (Japan)</li> </ul>	
	Immunity	<ul style="list-style-type: none"> <li>■ EN 61000-3-2 Power Line Harmonics</li> <li>■ EN 61000-4-2 ESD</li> <li>■ EN 61000-4-3 Radiated Immunity</li> <li>■ EN 61000-4-4 EFT</li> <li>■ EN 61000-4-5 Surge</li> <li>■ EN 61000-4-6 Low Frequency Common Immunity</li> <li>■ EN 61000-4-11 Voltage Dips and Sags</li> </ul>	
	NEBS	Designed to meet these standards; approval is pending <ul style="list-style-type: none"> <li>■ GR-63-Core: NEBS, Physical Protection</li> <li>■ GR-1089-Core: EMC and Electrical Safety for Network Telecommunications Equipment</li> <li>■ SR-3580 NEBS Criteria Levels (Level 3 Compliance)</li> </ul>	
	ETSI	<ul style="list-style-type: none"> <li>■ ETS-300386-2 Switching Equipment</li> </ul>	

## Ordering Information

Model Number	Description
<b>M20 Router</b>	
M20BASE-AC	M20 Base Unit: 4-slot chassis with cooling system, midplane, Routing Engine (768-MB DRAM, 80-MB flash drive, 6.4-GB hard drive, 110-MB flash PC card), two AC power supplies (AC power cables are country specific and sold separately), complete documentation (CD ROM)
M20BASE-DC	M20 Base Unit: 4-slot chassis with cooling system, midplane, Routing Engine (768-MB DRAM, 80-MB flash drive, 6.4-GB hard drive, 110-MB flash PC card), two DC power supplies, complete documentation (CD ROM)
<b>M20 Components</b>	
SSB-M20	System and Switch Board with Internet Processor ASIC
SSB-E-M20	Enhanced System and Switch Board with Internet Processor II ASIC
<b>M20 FPCs</b>	
FPC	Flexible PIC Concentrator
<b>M20 PICs</b>	
P-4E3	4-port E3 PIC (with cables)
P-4DS3	4-port DS-3 PIC (with cables)
P-4FE-TX	4-port Fast Ethernet PIC, TX interface with RJ45 connector
P-4OC3-SON-SMIR	4-port OC-3/STM-1 SONET/SDH PIC, single-mode, intermediate reach
P-4OC3-SON-MM	4-port OC-3/STM-1 SONET/SDH PIC, multimode
P-2OC3-ATM-SMIR	2-port OC-3/STM-1 ATM PIC, single-mode, intermediate reach
P-2OC3-ATM-MM	2-port OC-3/STM-1 ATM PIC, multimode
P-1OC12-SON-MM	1-port OC-12c/STM-4 SONET/SDH PIC, multimode
P-1OC12-SON-SMIR	1-port OC-12c/STM-4 SONET/SDH PIC, single-mode, intermediate reach
P-1CHOC12-DS3-SMIR	1-port Channelized OC-12 (SONET) to DS-3 PIC, single-mode, intermediate reach
P-1OC12-ATM-SMIR	1-port OC-12/STM-4 ATM PIC, single-mode, intermediate reach
P-1OC12-ATM-MM	1-port OC-12/STM-4 ATM PIC, multimode
P-1GE-LX	1-port Gigabit Ethernet PIC, LX Optics
P-1GE-SX	1-port Gigabit Ethernet PIC, SX Optics
I-1OC48-SON-SMIR	1-port OC-48c/STM-16 SONET/SDH interface (quad-wide PIC plus FPC), single-mode, intermediate reach
P-TUNNEL	Tunnel Services PIC
<b>M20 Power Cables</b>	
CBL-M20-PWR-AU	M20 AC power cable, Australia (10A, 8.2 ft / 2.5 m)
CBL-M20-PWR-EU	M20 AC power cable, Europe (10A, 8.2 ft / 2.5 m)
CBL-M20-PWR-IT	M20 AC power cable, Italy (10A, 8.2 ft / 2.5 m)
CBL-M20-PWR-JP	M20 AC power cable, Japan (10A, 8.2 ft / 2.5 m)
CBL-M20-PWR-UK	M20 AC power cable, UK (10A, 8.2 ft / 2.5 m)
CBL-M20-PWR-US	M20 AC power cable, US (10A, 8.2 ft / 2.5 m)
<b>M20 System Software</b>	
JUNOS	JUNOS Internet software (flash PC card) for USA and Canada (not for export)
JUNOS-WW	JUNOS Internet software (flash PC card) for all countries except the USA and Canada (satisfies USA government requirements for the export of encryption technology)
<b>M20 Documentation</b>	
<i>(Note: Complete CD ROM documentation ships with the base unit and is available online at <a href="http://www.juniper.net">http://www.juniper.net</a>)</i>	
DOC-M20-HW-S	Printed M20 hardware installation guide
DOC-JUNOS-S	Printed JUNOS software configuration guide
DOC-CD-S	Complete Juniper Networks documentation set on CD ROM



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